This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-49 (canceled)

Claim 50 (new): An apparatus for performing parity check message passing decoding operations, the apparatus comprising:

a message source for supplying at least one set of Z K-bit messages from any of at least L sets of Z K-bit messages, where Z is a positive integer greater than one and K and L are non-zero positive integers;

a node processor including a plurality of node processing units, each node processing unit for performing at least one of a parity check constraint node processing operation and a parity check variable node processing operation; and

a switching device coupled to the message source and to the node processing unit, the switching device for passing sets of Z K-bit messages between said message source and said node processor and for re-ordering the messages in at least one of said passed sets of messages in response to switch control information.

Claim 51 (new): The apparatus of claim 50,

wherein said message source is a memory device; and

wherein each of said plurality of node processing units is a variable node processing unit.

Claim 52 (new): The apparatus of claim 50, further comprising:

a message ordering control module coupled to said switching device for generating said switch control information used to control the reordering of messages in said at least one set of messages.

Claim 53 (new): The apparatus of claim 52, wherein the switching device includes circuitry for performing a message rotation operation to reorder messages included in a set of messages.

Claim 54 (new): The apparatus of claim 52, wherein the message ordering control module stores information on the order sets of messages are to be received from said message source and information indicating what reordering of messages is to be performed by said switch on individual sets of messages received from said message source.

Claim 55 (new): The apparatus of claim 52, wherein the message ordering control module is further coupled to said message source and sequentially generates set identifiers, each set identifier controlling the message source to output a set of messages.

Claim 56 (new): The apparatus of claim 55, wherein each set identifier includes a single memory address.

Claim 57 (new): The apparatus of claim 52, wherein said plurality of node processing units includes Z node processing units arranged in parallel, each one of the Z node processing units operating in parallel to process a different message in each set of Z messages passed between said message source and said node processor.

Claim 58 (new): The apparatus of claim 57, wherein said message source includes an identifier input which allows each set of messages to be addressed as a unit.

Claim 59 (new): The apparatus of claim 57, wherein each of said plurality of node processing units performs a variable node processing operation.

Claim 60 (new): The apparatus of claim 57, wherein the decoder control device is further coupled to said message ordering control module.

Claim 61 (new): The apparatus of claim 52, further comprising a decoder control module coupled to the message ordering module, the decoder control module including means for supplying information to the message ordering module used to control the order in which each of the L sets of Z messages are output by said message source.

Claim 62 (new): The apparatus of claim 61, further comprising a degree memory coupled to the node processor for storing a set of node degree information.

Claim 63 (new): The apparatus of claim 62, wherein the control device further generates a node index used to determine which node degree information in the stored set of node degree information is to be supplied to the node processor at any given time.

Claim 64 (new): The apparatus of claim 50, further comprising:
a second node processor coupled to said message source, the second node processor including a second plurality of node processing units, each of the second plurality of node processing units for performing constraint node processing operation.

Claim 65 (new): The apparatus of claim 64, further comprising:
a parity check verifier, coupled to said first node processor, for determining from an output of each of the first plurality of processing units included therein, when a parity check decoding operation has been successfully completed.

Claim 66 (new): A method of performing parity check message passing decoding processing comprising the steps of:
maintaining L sets of k-bit messages in a message storage device, each set of K-bit messages including first through Z messages, where L and Z are positive integers greater than one and K is a non-zero positive integer;

outputting one of said sets of K-bit messages from the message storage device;

performing a message reordering operation on said read set of K-bit messages to produce a reordered set of Z K-bit messages; and

supplying, in parallel, the Z messages in the reordered set of messages to a vector processor; and operating the vector processor to perform parity check message passing decoder operations using the Z supplied messages as input.

Claim 67 (new): The method of claim 66, further comprising: generating a message set identifier indicating the set of Z messages to be output by the message storage device.

Claim 68 (new): The method of claim 67, wherein the step of outputting one of said sets of K-bit messages includes: performing a SIMD output operation using said message set identifier to identify the set of messages to be output.

Claim 69 (new): The method of claim 66, further comprising: performing a second message reordering operation, the second message reordering operation being performed on the generated set of Z decoder messages to produce a reordered set of generated decoder messages.

Claim 70 (new): The method of claim 69, wherein the step of performing a second message reordering operation includes performing the inverse of the message reordering

operation performed on said set of K-bit messages output by the message storage device.

Claim 71 (new): The method of claim 70, wherein said message reordering operation is performed as a function of message set permutation information that includes cyclic rotation information.

Claim 72 (new): The method of claim 66, further comprising:

accessing stored message set permutation information; and

wherein the step of performing a message reordering operation includes the step of:

performing said reordering as a function of the accessed stored message set permutation information.

Claim 73 (new): The method of claim 66,

wherein said parity check message passing decoder operations are variable node low density parity check processing operations, each variable node processing operation including generating a decision value, and

wherein the method further comprises:

examining decision values generated by operating the vector processor to determine if a decoding condition has been satisfied.

Claim 74 (new): A method of performing parity check message passing decoding processing, the method comprising the steps of:

operating a variable node vector processor to

generate a set of Z K-bit messages, where Z is a positive integer greater than one and K is a non-zero positive integer; and

performing a message reordering operation on the generated set of Z K-bit messages to produce a reordered set of Z K-bit messages.

Claim 75 (new): The method of claim 74, wherein the step of operating the node vector processor to generate a set of Z K-bit messages, includes the step of:

performing, in parallel, Z node processing operations, each node processing operation generating one message in said set of Z K-bit messages.

Claim 76 (new): The method of claim 75, wherein performing a message reordering operation on the generated set of Z K-bit messages includes:

rotating the messages in the set of Z K-bit messages by performing a switching operation to reorder the messages in the set of messages.

Claim 77 (new): A method of performing parity check decoder operations, the method comprising:

performing a message output operation to output a set of messages;

performing a message reordering operation on the output set of messages to produce a reordered set of messages;

supplying the reordered set of messages to a node processor including a plurality of variable node processing units arranged in parallel; and

operating the plurality of variable node